AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS:

1. (Canceled).

2. (Canceled).

3. (Canceled).

4. (Canceled).

5. (Canceled).

6. (Canceled).

7. (Canceled).

8. (Canceled).

9. (Canceled).

10. (Canceled).

11. (Canceled).

12. (Original) A method for forming a variable capacitor, comprising:

depositing a first layer of an electrically conductive material on a substrate;

depositing a release layer formed of an electrically insulating material on a portion of the first electrically conductive layer;

depositing a second layer of an electrically conductive material on at least a portion of the release layer;

under-cut etching a portion of the release layer under the second layer to release a free portion of the second layer from the release layer, wherein an anchor portion of the second layer remains fixed to the release layer;

wherein the inherent stress profile in the second layer biases the free portion of the patterned second layer away from the release layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and the second layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer.

13. (Original) The method of claim 12, further comprising the step of depositing a dielectric layer between the release layer and the first electrically conductive layer.

14. (Original) The method of claim 12, further comprising the step of patterning the second electrically conductive layer into a spring shape prior to the under-cut etch step.

15. (Original) The method of claim 12, further comprising the step of patterning the second electrically conductive layer into a plurality of spring shapes.

16. (Canceled)

17 (Currently Amended) A method of forming a variable capacitor, comprising:

depositing a first layer of an electrically conductive material on a substrate;

depositing a release layer formed of an electrically insulating material on a portion of the first electrically conductive layer;

depositing a second layer of an electrically conductive material on at least a portion of the release layer;

patterning the second layer into a capacitor plate layer and a microcoil layer;

under-cut etching a portion of the release layer under the second layer to release a free portion of the capacitor plate layer and the microcoil layer from the release layer, wherein an anchor portion of the capacitor plate layer remains fixed to the release layer;

wherein the inherent stress profile in the second layer biases the free portion of the capacitor layer away from the release layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and the second layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer;

wherein the intrinsic stress profile in the microcoil layer biases the free portion of the microcoil layer away from the substrate, forming a loop winding and causing a free end to contact a point on the substrate; and

connecting the free end to the substrate.